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TUCKER, ELLIS & WEST LLP
1150 HUNTINGTON BUILDING
925 EUCLID AVENUE
CLEVELAND, OH 44115-1414

EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/607,815	BATCHER, KENNETH W.	
	Examiner	Art Unit	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-11,14,15,17,23,24 and 26-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-11,14,15,17,23,24 and 26-32* is/are rejected.

7)☒ Claim(s) *33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Fritz M. Fleming
FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
Supervisory 4/4/2006
AU 2181

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 1, 2006 has been entered.

Claim Objections

2. Claim 10 is objected to because of the following informalities: In claim 10, line 18, the limitation "means for" has been duplicated. Please delete the extra "means for" limitation. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 7-11, 14-15, 17, 23, 24, and 26-32 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Masse et al., US Patent Application Publication 2003/0093656 (herein referred to as Masse).

5. Referring to claims 1 and 8, Masse has taught a method of operating a processor to repeatedly execute an instruction;

a. determining at run time how many times a single instruction is to repeated (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], Figure 10, page 6, paragraph [0086]-page 7, paragraph [0098]);

b. loading at run time an existing general purpose register with a count value indicative of the number of times the single instruction is to be executed (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, elements 922 and 902);

c. fetching and executing a REPEAT instruction, the REPEAT instruction indicating the single instruction to be repeatedly re-executed (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 11, element 1102);

d. fetching the single instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 11, element 1108a, AC0); and

e. repeatedly executing the single instruction for a consecutive number of times as indicated by the count value and without adding a NOP (no operation) instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], specifically see paragraph [0096]);

f. adjusting the count value in the register each time the single instruction is executed (Figure 10, element 924, page 7, paragraph [0092-0096], Figure 11, element 922, page 7, claim 9)

g. wherein adjusting the count value only operates while the means for repeatedly executing the single instruction is executing the single instruction (Figure 10, elements 922 and 924, page 7, paragraph [0091-0096], Figure 11, element 922, page 7, claim 9, page 1, paragraph [0009-0011] and [0018], page 2, paragraph [0020], page 4, paragraph [0053]).

6. Referring to claim 2, Masse has taught a method of operating a processor to repeatedly execute a single instruction and to repeatedly execute a block of instructions,

a. fetching a REPEAT instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 11, element 1102);

b. executing a REPEAT instruction, wherein execution of the REPEAT instruction determines and stores at run time in an existing general purpose register a count value indicative of the number of times a single instruction is to be executed (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], elements 902 and 922, Figure 11, element 1102);

c. fetching the single instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph

[0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 11, AC0 at 1108a); and

d. repeatedly executing the single instruction consecutively for as many times as indicated by the count value without re-fetching the single instruction and without fetching any other instruction and without adding a NOP (no operation) instructions (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 11, AC0 at 1108a is repeated in accordance with k in the loop counter.);

e. decrementing the count value in the register each time the single instruction is executed (Figure 10, element 924);

f. incrementing a program counter once the count value in the register is one of less than zero and equal to zero, thereby providing an effective data rate of one transfer every clock cycle (page 7, paragraphs [0096] [0097]);

g. wherein decrementing the count value in the register does not start until repeatedly executing the single instruction begins (Figure 10, elements 922 and 924, page 7, paragraph [0091-0096], Figure 11, element 922, page 7, claim 9, page 1, paragraph [0009-0011] and [0018], page 2, paragraph [0020], page 4, paragraph [0053]).

7. Referring to claim 3, Masse has taught a method of operating a processor to repeatedly execute a single instruction and to repeatedly execute a block of instructions (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056]),

a. determining at run time a count value indicative of how many times a single instruction is to repeated (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056]);

b. loading at run time a general purpose register with the count value indicative of the number of times a single instruction is to be executed (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 10, elements 902 and 922);

c. fetching and executing a REPEAT instruction indicating the single instruction that is to be repeatedly executed (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 11, element 1102);

d. incrementing a program counter (Figure 10, element 924, page 7, paragraph [0097]);

e. fetching the single instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 11, element 1108a, AC0); and

f. repeatedly executing the single instruction for as many times as indicated by a count value stored in the count register without re-fetching the single instruction and without fetching any other instruction and without adding a NOP (no operation)

instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056]);

g. decrementing the count value in the register each time the single instruction is executed (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], page 4, left column, paragraphs [0053]-[0056], Figure 10, element 924);

h. stalling the program counter once the count value in the register is one of less than zero and equal to zero, thereby providing an effective data rate of one transfer every clock cycle (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], page 4, left column, paragraphs [0053]-[0056], Figure 10, page 3, paragraph [0050]-page 6, paragraph [0085]);

i. wherein decrementing the count value in the register does not start until repeatedly executing the single instruction begins (Figure 10, elements 922 and 924, page 7, paragraph [0091-0096], Figure 11, element 922, page 7, claim 9, page 1, paragraph [0009-0011] and [0018], page 2, paragraph [0020], page 4, paragraph [0053]).

8. Referring to claim 4, Masse has taught the method of operating a processor according to claim 3, as described above, wherein said count value is stored in said count register before execution of said REPEAT instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 10, elements 902 and 922).

9. Referring to claim 7, Masse has taught the method according to claim 3, as described above, wherein method further comprises: decrementing said count value stored in said register each time said associated instruction is executed; and determining whether said count value is less than or equal to zero (Figure 10, element 924).

10. Referring to claim 9, Masse has taught a processor for repeatedly executing a single instruction and to repeatedly execute a block of instructions,

a. means for determining at run time how many times a single instruction is to be repeated (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056]);

b. means for fetching a REPEAT instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 11, element 1102);

c. means for executing a REPEAT instruction, wherein execution of the REPEAT instruction at run time stores in a general purpose register a count value indicative of the number of times the instruction is to be executed (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], elements 902 and 922);

d. means for fetching the single instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page

7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 11, element 1108a, AC0); and

e. means for repeatedly executing the single instruction for as many times as indicated by the count value without re-fetching the single instruction and without fetching any other instruction without adding a NOP (no operation) instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056]);

f. means for decrementing the count value in the register each time the single instruction is executed (Figure 10, element 924);

g. means for incrementing a program counter once the count value in the register is less than zero, thereby providing an effective data rate of one transfer every clock cycle (page 7, paragraph [0097]);

h. wherein the means for decrementing only operates while the means for repeatedly executing the single instruction is executing the single instruction (Figure 10, elements 922 and 924, page 7, paragraph [0091-0096], Figure 11, element 922, page 7, claim 9, page 1, paragraph [0009-0011] and [0018], page 2, paragraph [0020], page 4, paragraph [0053]).

11. Referring to claim 10, Masse has taught a processor for repeatedly executing a single instruction and to repeatedly execute a block of instructions (Masse, column 2 line 20-column 4, line 12, figures 1 and 2),

a. means for determining at run time how many times a single instructions is to be repeated (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056]);

b. means for loading a general purpose register at run time with a count value indicative of the number of times a single instruction is to be executed (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], elements 902 and 922);

c. means for fetching a REPEAT instruction indicating the single instruction that is to be repeatedly executed; (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 11, element 1102, Figure 11, element 1102);

d. means for executing the REPEAT instruction indicating the single instruction that is to be repeatedly executed without adding a NOP (no operation) instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 11, element 1102);

e. means for incrementing a program counter (page 7, paragraph [0097]);

f. means for fetching the single instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page

7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 11, element 1108, Figure 11, element 1108a, AC0); and

g. means for repeatedly executing the single instruction for a consecutive number of times as indicated by a count value stored in a count register without re-fetching the single instruction and without fetching any other instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056]);

h. means for decrementing the count value in the register each time the single instruction is executed (Figure 10, element 924);

i. means for incrementing a program counter once the count value in the register is one of less than zero and equal to zero, thereby providing an effective data rate of one transfer every clock cycle (page 7, paragraph [0097]);

j. wherein the means for decrementing only operates while the means for repeatedly executing the single instruction is executing the single instruction (Figure 10, elements 922 and 924, page 7, paragraph [0091-0096], Figure 11, element 922, page 7, claim 9, page 1, paragraph [0009-0011] and [0018], page 2, paragraph [0020], page 4, paragraph [0053]).

12. Referring to claim 11, Masse has taught a processor according to claim 10, as described above, wherein said count value is stored in said count register before execution of said REPEAT instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph

[0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 10, elements 902 and 922).

13. Referring to claim 14, Masse has taught a processor according to claim 10, as described above, wherein processor further comprises:

a. means for determining whether said count value is less than or equal to zero (Figure 10, element 926).

14. Referring to claim 15, Masse has taught a processor for repeatedly executing one or more processor instructions (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056]), comprising:

a. a memory address register associated with a main memory (Figures 5 and 7, page 1, paragraph [0006], page 2, paragraph [0037], page 3, paragraphs [0042] [0043] [0050], page 4, paragraph [0054] [0060] [0061]);

b. a memory control for generating memory control signals (Figure 1, element 104, page 1, paragraph [0006], page 2, paragraph [0037], page 3, paragraphs [0042] [0043] [0050], page 4, paragraph [0054] [0060] [0061]);

c. a program counter for storing a memory address location of the main memory where an instruction is to be fetched (Figures 5 and 7, page 1, paragraph [0006], page 2, paragraph [0037], page 3, paragraphs [0042] [0043] [0050], page 4, paragraph [0054] [0060] [0061]);

d. an instruction register for storing an instruction that is to be executed (page 2, paragraph [0037], page 3, paragraph [0050], elements 106 and 502);

e. at least one general purpose register storing a count (Figure 10, elements 902 and 922);

f. decode and execute control logic for decoding and executing an instruction stored in the instruction register (page 4, Figure 5, P2-P6); and

g. a state machine for controlling the fetching and repeated execution of a single instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056], Figure 11, element 1108a, AC0);

h. the state machine configured to repeatedly execute the single instruction by signaling the instruction register to hold the same instruction and to fetch the next instruction (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], Figure 10, page 4, left column, paragraphs [0053]-[0056]); and

i. decrement the count stored in the register each time the single instruction is executed (Figure 10, element 924), and

j. signal the program counter not to increment until the count value stored in the general purpose register is below a threshold value, thereby providing an effective data rate of one transfer every clock cycle (page 7, paragraphs [0096] [0097]);

k. wherein the state machine only decrements the count stored in the general purpose register while the single instruction is executed (Figure 10, elements 922 and 924, page 7, paragraph [0091-0096], Figure 11, element 922, page 7, claim 9, page 1, paragraph [0009-0011] and [0018], page 2, paragraph [0020], page 4, paragraph [0053]).

15. Referring to claim 17, Masse has taught the processor according to claim 15, as described above, wherein said general purpose register includes a first register for storing a count value indicative of the number of times the one or more associated instructions are to be repeatedly executed (Figure 10, elements 902 and 922).

16. Referring to claim 26, Masse has taught the processor of claims 8, as described above, and further comprising means for incrementing a program counter once the count value is equal to zero (page 7, paragraph [0097]).

17. Referring to claims 23, 24 and 27, Masse has taught the processor of claims 8 and 15, as described above, and further comprising the state machine configured to increment the program counter once the count value is less than zero (page 7, paragraph [0097]).

18. Referring to claims 28, 29 and 31, Masse has taught the processor according to claims 15, 8, and the method of operating a processor according to claims 2 and 3, as described above, wherein the program counter remains unchanged as the single instruction is repeatedly executed (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], page 4, left column, paragraphs [0053]-[0056], Figure 10, page 3, paragraph [0050]-page 6, paragraph [0085]).

19. Referring to claims 30 and 32, Masse has taught the method of operating a processor according to claims 2 and 3, as described above, wherein the program counter is effectively stalled on the single instruction until the single instruction executes the number of times indicated by the count value (abstract, page 1, right column, paragraph [0008]-page 2, left column, paragraph [0019], page 6, paragraph [0086]-page 7, paragraph [0098], page 4, left

column, paragraphs [0053]-[0056], Figure 10, page 3, paragraph [0050]-page 6, paragraph [0085]).

Response to Arguments

20. Applicant's arguments filed February 1, 2006 with respect to claims 1-4, 7-11, 14, 15, 17, 23, 24, 26-32 have been fully considered but they are not persuasive.

21. On pages 10 and 11, Applicant argues in essence:

> *"The loop counter in Masse "is tested, decremented and updated during the address stage P3 of the pipeline" (0096). "When the single repeat instruction has terminated, i.e. loop counter 922 value=0 at 1110, the rest of the repeat block is executed" (Id.). Because of this, Masse has a latency of four instruction cycles (0094). In other words, the counter is being decremented before the single instruction to be executed has started executing. Referring to annotated Figure 11 attached hereto, during the third clock cycle (T3) the counter begins to decrement. When the instruction finally begins to execute at the sixth clock cycle (T6), the counter has already reached 0. Whereas, as now claimed by claims independent claims 1-3, 8-10 and 15 the counter is not decremented until the instruction is being executed, and is decremented (or adjusted) each time the instruction executes."*

However, Examiner respectfully points out that the repeat instruction is executed by modifying the repeat count register (see page 1, paragraphs [0009-0011]). Processors execute instructions in a pipeline. In the case of Masse instructions are executed through a 7 stage pipeline (page 4, paragraph [0053]). The address stage is a part of the instruction execution (page 4, paragraph [0058]). Therefore, the fact that the repeat counter register of Masse may be decremented during the address stage does not differ from the claimed invention because the address stage is a part of instruction execution. Therefore this argument is moot.

Allowable Subject Matter

22. Claim 33 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, with every other Friday off.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

Fritz M. Fleming

FRITZ FLEMING
Supervisory PRIMARY EXAMINER
GROUP 2100
AU 2181

4/14/2006